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APPLICATION FOR LETTERS PATENT

TITLE: CHANNEL DECODER FOR A DIGITAL BROADCAST  
RECEIVER

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### Description

- 1 The present invention relates to a channel decoder for a digital broadcast receiver, in particular to the use of the packet synchronization status available within such a channel decoder, i. e. within the synchronization byte detector included in such a channel decoder. In this sense the packet synchronization  
5 status indicates the lock-in of the receiver to one broadcast channel.

The typical hardware structure of a channel decoder within a digital video broadcast receiver adapted to the satellite reception is shown in Fig. 3. The IF-signal generated by the tuner of the digital broadcast receiver is supplied to a  
10 baseband conversion circuit 8 that receives at a second input thereof a control signal supplied by a control circuit 9. The demodulated signal is then supplied to the channel decoder before it passes a baseband physical interface 10 that outputs a transport stream of data.

- 15 In the shown example of satellite reception, the channel decoder includes as a first stage a baseband filtering & clock/carrier recovery circuit 2 which supplies a feedback signal to the control circuit 9. The baseband filtering & clock/carrier recovery circuit 2 includes a not shown clock and carrier recovery loop comprising clock/carrier phase detectors which is usually built by a PLL circuit to gain the clock and carrier of the transmitted signal. The resulting de-  
20 modulated and baseband filtered IF-signal gets decoded in a Viterbi-decoder 5 which outputs a bitstream of the decoded bits of the transmission signal. This bitstream undergoes an error correction by a forward error correction (FEC) which is built by a de-interleaver 3 followed by a Reed-Solomon decoder 6 and  
25 an energy dispersal removal circuit 7 before being output to the baseband physical interface 10.

- The de-interleaver 3, the RS-decoder 6 and the energy dispersal removal circuit 7 need synchronization signals that indicate transport stream packets as well as an 8-packet-structure for the energy dispersal removal. The synchroni-  
30 zation signals are generated by a sync-byte-detector 1 which detects the regular repeated transmission of the synchronization byte (0x47 in the MPEG transport packet structure) or it is inverted (0xb8 in the MPEG transport packet structure) every 1632 bits (204 bytes).

- 1 Depending whether such a receiver is used for transmission signals  
transmitted via satellite, via cable or via a terrestrial broadcasting an  
additional signal processing might be necessary within the processing stages  
of the receiver described above. The basic differences of channel decoders  
5 adapted to the different kinds of broadcasting are described hereinafter in con-  
nection with an embodiment according to the present invention.

Also, the channel decoder of DAB receiver is in its main parts identical to the  
channel decoder described above and shown in Fig. 3, i.e. it also comprises a  
10 clock/carrier recovery circuit, a sync-byte-detector and a FEC-stage.

It is the object underlying the present invention to provide an improved chan-  
nel decoder for a digital broadcast receiver.

- 15 This object is solved with a channel decoder for a digital broadcast receiver ac-  
cording to the present invention which comprises a synchronization byte de-  
tector 1 and which is characterized in that said synchronization byte detector  
1 provides an output signal indicating the lock-in of the receiver to one broad-  
cast channel which is used as a feed forward and/or feedback signal to respec-  
20 tively switch processing stages succeeding and/or preceding said synchroniza-  
tion byte detector 1 into a different mode dependent on whether or not lock  
has been achieved.

- Preferable embodiments of the present invention are defined in dependent  
25 claims 2 to 8, respectively.

- The use of the lock detected signal not only for purposes within the sync-byte-  
detector, but also to provide it within the whole channel decoder or even pro-  
vide it to the whole broadcast receiver to switch processing stages into differ-  
30 ent modes, e. g. to switch-off all stages following the synchronization byte de-  
tector in the signal flow in case of an unlocked state, leads to less power con-  
sumption of the receiver and to less CPU resources needed within the receiver,  
since the dynamic assignment of CPU resources dependent on the synchroni-  
zation status becomes possible.

- 35 According to the prior art the error correction stage operates in worst case  
condition if an incoming packet is not correctable, i. e. if the receiver is in un-

1 locked state, and therewith exhibits a high power consumption and needs a  
high amount of CPU resources. Therefore, especially the switching of process-  
ing stages preceding and succeeding the synchronization byte detector depend-  
ent on whether or not lock has been achieved according to the present inven-  
5 tion enables the shifting of processing power from the error correction stages  
succeeding the synchronization byte detector to the clock and/or carrier recov-  
ery during acquisition of a broadcast channel and vice versa if the receiver is  
properly locked to a broadcast channel. With this measure processing power is  
saved during acquisition of a broadcast channel, since the forward error  
10 correction and preferably all further following processing stages get switched-  
off in case the receiver is not locked to a certain broadcast channel.

Furtheron, if the loop bandwidth of the clock and carrier recovery loop built  
within the baseband filtering & clock/carrier recovery circuit gets switched de-  
15 pendent on whether or not lock has been achieved the baseband filtering &  
clock/carrier recovery circuit needs less calculation power after the receiver is  
locked, since only a narrow bandwidth has to be processed in this case.

It is also possible to switch the loop bandwidth of other loops preceding the  
20 sync-byte detector i. e. g. of a loop that adjusts the tuning frequency of the re-  
ceiver.

For these reasons, the present invention inherits the advantage that a smaller  
CPU can be built into a digital broadcast receiver which comprises a channel  
25 decoder according to the present invention, since after the lock-in to a broad-  
cast channel the spare processing power of the baseband filtering & clock/car-  
rier recovery circuit and/or any other circuit that is preceding the sync-byte-  
detector can be shifted to the forward error correction stage and the process-  
ing stages following thereafter. Vice versa, if the broadcast receiver adapted  
30 according to the present invention is not locked to a broadcast channel a high  
processing power can be assigned to the baseband filtering & clock/carrier re-  
covery circuit and/or any other circuit that is preceding the sync-byte-detec-  
tor, since the forward error correction stage and the processing stages follow-  
ing thereafter need no processing power at all.

35 Still furtheron, the digital broadcast receiver according to the present  
invention achieves a better reconstruction of the transmitted data, since the  
clock and/or carrier phase detectors used within the baseband filtering &

- 1 clock/carrier recovery circuit can be switched to implementations that work  
only in locked mode, but in this case better than the robust implementations  
used for acquisition, dependent on the synchronization status of the channel  
decoder, i. e. the sync-byte-detector. Such a switching is also thinkable for  
5 other circuits within the broadcast receiver.

The present invention is in particular applicable to digital video broadcast  
receivers and in particular to such for cable transmission, but it can also be  
used for satellite or terrestrial transmission and/or for digital audio broadcast  
10 reception according to any transmission standard. Basically, it can be imple-  
mented in any channel decoder.

An exemplary embodiment of the present invention will be described in  
connection with the accompanying figures in which

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**Fig. 1** shows a block diagram of a channel decoder according to a preferred  
embodiment of the present invention;

**Fig. 2** shows the basic differences inbetween receivers for the satellite, the  
cable and the terrestrial broadcast system.

20 **Fig. 3** shows a block diagram of the signal processing within a digital video  
broadcast receiver according to the prior art, in particular within its  
channel decoder.

From a signal flow point of view the channel decoder according to the present  
25 invention shown in Fig. 1 basically works in the same way as the channel de-  
coder described in connection with Fig. 3. According to the present invention  
the sync-byte-detector 1 included within the channel decoder according to the  
present invention additionally generates a lock detected output signal which  
indicates the lock-in to a specific broadcast channel. This lock detected output  
30 signal is supplied to at least one of the clock/carrier recovery circuit 2, the de-  
interleaver 3, the RS-decoder 6, the energy dispersal removal circuit 7 and an  
additional output port 4 of the channel decoder.

As described above, on basis of the lock-detected output signal of the sync-  
35 byte-detector 1 the clock/carrier recovery circuit 2 is able to switch the loop  
bandwidth of its clock and/or carrier recovery loop and/or to switch the clock  
carrier phase detectors to implementations that work only in locked mode, but  
in this case better than the robust implementation used for acquisition.

1 Furtheron, the de-interleaver 3, the Reed-Solomon-decoder 6 and the energy  
dispersal removal circuit 7 receive the lock detected output signal of the sync-  
byte-detector 1 at a respective enable input so that they can be switched-on if  
lock has been achieved and switched-off in unlocked state.

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Furtheron, the lock detected output signal of the sync-byte-detector 1 is  
supplied to an additional output port 4 of the channel decoder so that also  
other processing stages within the digital broadcast receiver can be switched  
into different modes for an improved power consumption and/or processing  
10 power consumption of the whole digital broadcast receiver like it is performed  
within the channel decoder according to the present invention.

Fig. 1 shows that the lock detected output signal is also supplied to an enable  
input of the baseband physical interface 10 that is arranged succeeding the  
15 channel decoder according to the present invention. Therefore, also this base-  
band physical interface 10 gets switched-on if lock has been achieved and  
switched-off in unlocked state. Furtheron, also the controller 9 receives the  
lock detected output signal via the output port 4 so that all processing stages  
within the receiver that are connected to the controller 9 might be included in  
20 the dynamic assignment of processing power. In the shown example the base-  
band conversion circuit 8 receives a control signal from the controller 9 and  
therefore a loop which is build by the baseband filtering & clock/carrier recov-  
ery circuit 2, the controller 9 and the baseband conversion circuit 8 to prop-  
erly adjust the baseband conversion can e. g. be switched in view of its band-  
25 width and/or adjusting strategies.

Fig. 2 shows that a "digital demodulator" which comprises a baseband conver-  
sion stage 8, a baseband filtering & clock/carrier recovery circuit 2 and a Vit-  
erbi-Decoder 5 in case of satellite reception, as shown in Figs. 1, 3 and 2a,  
30 comprises a baseband conversion stage 8b, a baseband filtering & clock/car-  
rier circuit 8b and an adaptive equalizer 5b in case of cable reception as it is  
shown in Fig. 2b and that it comprises a baseband conversion stage 8c, a  
COFDM demodulator & clock/carrier recovery circuit 2c and a Viterbi-decoder  
5c in case of terrestrial reception as it is shown in Fig. 2c. The COFDM de-  
35 modulator performs an IFFT, i. e. an inverse fast Fourier transformation.

In the shown examples the processing stages corresponding to those shown  
and described in connection with Fig. 1 get switched in the same or an equal

- 1 manner on basis of the lock detected output signal supplied by the sync-byte-detector.

The adaptive equalizer 5b shown in Fig. 2b also receives the lock detected out-  
5 put signal to change its adaptation strategy dependet therefrom from an acquisition mode to a tracking mode in case of lock-in of the receiver and vice-versa in case the receiver is not locked-in. Of course, this changing of the adaptation strategy is not limited to adaptive equalizers within channel decoders used in case of cable reception.

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The channel decoder of the typical digital audio receiver locks basically as the one shown in Figs. 1 and 3 in connection with the "digital demodulator" shown in Fig. 2c and can of course also be replaced by a channel decoder according to the present invention which uses a lock detected signal output by its syn-  
15 chronization-byte-detector to dynamically assign processing power to different processing units within the channel decoder and/or also the rest of the digital audio broadcast receiver.

From the above description it is clear that the invention is not limited to just  
20 disable/enable the error correction, to switch the loop bandwidth of the clock and carrier recovery loop and/or to switch the clock carrier phase detectors to implementations that work only in locked mode, but in this case better than the robust implementations used for acquisition, but that the present invention discloses the use of the packet synchronization status, namely a lock  
25 detected signal supplied by the synchronization byte detector 1 to assign the amount of processing power within a digital broadcast receiver.

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